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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,056	07/11/2003	Peter Poechmueller	P03,0252	4318

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EXAMINER	
BATHINI JR, LEON M	
ART UNIT	**PAPER NUMBER**
2857	

DATE MAILED: 01/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,056	POECHMUELLER, PETER	
	Examiner	Art Unit	
	Leon M. Bathini Jr.	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/20/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-3, 7-12, and 15-16** are rejected under 35 U.S.C. 102(b) as being anticipated by Brown et al. (U.S. Patent Number 6,609,077 B1).

With respect to **claims 1-3 and 7-12**, Brown et al. teach the following:

- a device for calibrating signals, comprising of at least two signal circuits (22, 24, 28, 30) configured to generate signals (col. 3, lines 12-24); and evaluation-drive circuitry (40) configured to evaluate the signals generated by the signal circuits and that drives at least one of the signal circuits such that a time reference (col. 7, line 61- col. 8, line 2 and 9) of the signals generated by the signal circuits relative to one another is set corresponding to at least one prescribed value (col. 3, lines 24- 30).

- the evaluation-drive circuitry further comprises at least one comparator (32) that is allocated to the at least two signal circuits and that is configured to compare the signal generated by the at least two signal circuits to one another (col. 3, lines 20-24).

- the evaluation-drive circuitry further comprises a logic circuit (40) configured to evaluate an output signal of the at least one comparator (32) (col. 3, lines 41-44).

- the evaluation-drive circuitry further comprises at least one multiplexer (62) to which output signals of comparators are supplied (col. 4, lines 7-11).

- the multiplexer is controlled by a logic circuit (42) configured to evaluate an output signal of the at least one comparator (col. 4, lines 4-11).

- a signal generator configured to generate a reference signal with which the signals generated by the signal circuits can be calibrated (col. 4, lines 43-50). The reference signal is the incident edge.

- the reference signal that is generated by the signal generator is supplied to at least one comparator (col. 4, lines 43-50).

- the signal circuits are drivers (col. 3, lines 21-24).

- a semiconductor chip comprising the device (col. 6, lines 57-63). A semiconductor chip includes pin electronics circuitry. It can be inferred that the pin electronics circuitry can be made in a semiconductor chip.

With respect to **claims 15-16**, Brown et al. teach the following:

- a method for calibrating signals, comprising; providing at least two signal circuits (22, 24, 28-30) for generating signals (col. 3, lines 12-24); generating signals by the at least two signal circuits (col. 3, lines 12-24); evaluating the signals generated by the signal circuits and driving at least one of the at least two signal circuits such that a time reference (col. 7, line 61 – col. 8, lines 2 and 9) of the signals generated by the signal circuits relative to one another is set corresponding to at least one prescribed value (col. 3, lines 20-24).

- a method for comparing the signals generated by the at least two signal circuits to one another for the evaluation and producing a comparison result (col. 3, lines 20-24).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claim 4-6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al. in view of Burlison et al. (U.S. Patent No. 6,880,137 B1).

With respect to the above claims, Brown et al. teach at least one register (53) that is connected to a logic circuit (56) configured to evaluate an output signal of the at least one comparator (32) via a register bus (col. 4, lines 9-11), except that Brown et al. does not teach the elements in **claims 4-5**.

However, Burlison et al. teach the following elements in **claims 4-5**:

- the evaluation-drive circuitry further comprises at least one programmable delay loop, and a programmable delay loop (1315) that is allocated to at least one signal circuit (1305) in order to set a delay of the signal circuit (col. 6, lines 29-37).

- the evaluation-drive circuitry further comprises at least one register (1330) and a register in which a delay value can be stored is allocated to at least one programmable delay loop (col. 6, lines 37-43).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the ATE (automatic test equipment) timing and measuring unit of Brown et al. to include an evaluation-drive circuitry comprising of a programmable delay loop and register as taught by signal delay test system for ATE of Burlison et al., because having a register, wherein a programmable delay loop value can be stored, allows for a wider range of test data as well as facilitating the calibration of test signals to the device under test.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al. in view of Sugamori et al. (U.S. Patent No. 6,631,340 B2).

With respect to the above claims, Brown et al. teach all the features of the claimed invention, except that Brown et al. does not teach the elements in **claim 13.**

However, Sugamori et al. teach an ASIC comprising the device that is configured for testing dynamic memory modules (col. 8, lines 11-14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the ATE timing and measurement unit of Brown et al. to include a separate testing device configured for testing memory as taught by the semiconductor memory test system of Sugamori et

al., because having a separate testing device configured for testing memory allows for testing both memory and a logic devices simultaneously thereby being more efficient and cost effective.

5. **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al. in view of Maggi et al. (U.S. Patent No. 4,554,636).

With respect to the above claims, Brown et al. teaches all the features of the claimed invention, except that Brown et al. does not teach the elements in **claim 14.**

However, Maggi et al. teach a component for calibrating signals for performing a self-test on the component (col. 12, line 61 – col. 13, line 32).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the ATE timing and measurement unit of Brown et al. to include a self-test operation on the component as taught by the testing circuit apparatus of Maggi et al., because a self-test on the test equipment ensures accurate calibration of signals, which in return results in accurate measurements from test equipment.

6. **Claims 17-20,** are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al. in view of Niwa et al. (U.S. Patent No. 6,448,799 B1).

With respect to the above claims, Brown et al. teaches a method of driving, by the logic circuit, for the sequential evaluation of a plurality of comparison results, a multiplexer at whose inputs the comparison results are adjacent (col. 4, lines 7-11) as taught in **claim 20**, except that Brown et al. does not test the elements in **claims 17-19**.

However, Niwa et al. teach the following elements:

- a method of programming at least one of the signal circuits (21, 23-2n, and 93-94) dependent on the comparison result such that the signal it generates is delayed according to the prescribed value (col. 4, lines 11-23 and col. 3, lines 1-8). It is well known in the art that memory, which in this case consists of RAM modules contained in the control circuit, can be programmed and can thus store various data.

- a method for providing a logic circuit comprising an algorithm; and executing, by the algorithm, the evaluating and programming utilizing the prescribed value (col. 4, lines 3-9 and col. 3, lines 1-8). It is inherent that the algorithm is contained in the ROM or RAM of the control circuit (10) that executes an algorithmic value based on the prescribed value.

- a method for sequentially evaluating, by the logic circuit, a plurality of comparison results (col. 4, lines 10-23).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the ATE timing and measurement unit of Brown et al. to include a method of programming the delay circuit and for sequentially evaluating the comparison results by the logic circuit as taught by the timing adjustment method for semiconductor testing of Niwa et al., because a programmable signal circuit allows for more flexibility in the number of functions the signal circuit can do. Also evaluating the results sequentially as well as using a logic circuit comprising of an algorithm is what is generally used in conventional computers consisting of serial processors.

7. **Claims 21, and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al. in view of Burlison et al. (U.S. Patent No. 6,880,137 B1) and Niwa et al. (U.S. Patent No. 6,448,799 B1).

With respect to the above claims, Brown et al. in combination with Niwa et al. teach all the features of the claimed invention, except that Brown et al. in view of Niwa et al. do not teach the elements in **claims 21, and 22**.

However, Burlison et al. teach the following:

- a method wherein the programming comprises driving, by the logic circuit, at least one of at least two registers (1330 and 1335) via a register bus; and storing a delay value in the at least one register, the at least two registers being respectively allocated to the signal circuits (col. 6, lines 29-42).

- a method of reading the delay value stored in a register by a programmable delay loop that in turn programs a signal circuit according to the delay value that is read (col. 6, lines 29-42).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the ATE timing and measuring unit of Brown et al. to include an evaluation-drive

circuitry comprising of a programmable delay loop and register as taught by Burlison et al., because having a register, wherein a programmable delay loop value can be stored, allows for a wider range of test data as well as facilitating the calibration of test signals to the device under test.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon M. Bathini Jr. whose telephone number is 571-272-7129. The Examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Marc Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LBJ

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